PATENT

In re application of: Lescot, et al.

Attorney Docket No.: SNTCP001X2C1

Application No.: To Be Assigned

Examiner: To Be Assigned

Filed: July 12, 2001

Group: To Be Assigned

Title: APPARATUS FOR MODELING IC SUBSTRATE NOISE UTILIZING IMPROVED DOPING PROFILE ACCESS KEY

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on July 12, 2001 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number **EL898676775US**, addressed to the Commissioner for Patents, Washington, DC 20231.

Misha Eisman

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please amend the above-identified patent application as follows.

In the **SPECIFICATION**:

On page 1, line 7, please insert the following:

--Related Applications

This application is a continuation application of an earlier filed commonly owned patent application entitled "Method of Modeling IC Substrate Noises Utilizing Improved

Doping Profile Access Key" filed on March 27, 2000 (Serial No. 09/536,206), Attorney Docket No. SNTCP001X2, which is incorporated herein by reference for all purposes.

This application is also related to a commonly owned patent application entitled "Method for Modeling Noises in an Integrated Circuit" filed on March 4, 1999 (Serial No. 09/262,735), Attorney Docket No. SNTCP001.

This application is related to a commonly owned patent application entitled "IC Substrate Noise Modeling With Improved Surface Gridding Technique" filed on January 31, 2000 (Serial No. 09/495,078), Attorney Docket No. SNTCP001X1.

This application is also related to a commonly owned patent application entitled "IC Substrate Noise Modeling Including Extracted Capacitance for Improved Accuracy" filed on March 27, 2000 (Serial No. 09/536,256), Attorney Docket No. SNTCP001X3.

This application is also related to a commonly owned patent application entitled "Apparatus for Modeling Noises in an Integrated Circuit" filed on July 11, 2001 (Serial No. _____), Attorney Docket No. SNTCP001C1.--

In the **CLAIMS**:

Please **ADD** the following claims:

2. A computer-readable medium storing thereon computer-readable instructions configured for characterizing an integrated circuit substrate, comprising:

instructions for obtaining a substrate doping profile, the substrate doping profile including a net doping level for each one of a plurality of depths within the integrated circuit substrate;

instructions for vertically discretizing the substrate doping profile to form a vertically discretized substrate doping profile; and

instructions for associating the vertically discretized doping profile with an access key, the access key comprising a region name and a cross-section name.

3. The computer-readable medium as recited in claim 2, wherein the region name corresponds to a region of the integrated circuit substrate.

4. The computer-readable medium as recited in claim 3, wherein the region of the integrated circuit substrate is defined by a horizontal area of the integrated circuit substrate.

5. The computer-readable medium as recited in claim 2, wherein the cross-section name corresponds to a cross-section of the integrated circuit substrate.

6. The computer-readable medium as recited in claim 5, wherein the cross-section of the integrated circuit substrate is defined by a vertical area of the integrated circuit substrate.

7. An apparatus for characterizing an integrated circuit substrate, comprising:

means for obtaining a substrate doping profile, the substrate doping profile including a net doping level for each one of a plurality of depths within the integrated circuit substrate;

means for vertically discretizing the substrate doping profile to form a vertically discretized substrate doping profile; and

means for associating the vertically discretized doping profile with an access key, the access key comprising a region name and a cross-section name.

8. An apparatus for characterizing an integrated circuit substrate, comprising:

a processor; and

a memory, at least one of the processor and the memory being adapted for:

obtaining a substrate doping profile, the substrate doping profile including a net doping level for each one of a plurality of depths within the integrated circuit substrate;

vertically discretizing the substrate doping profile to form a vertically discretized substrate doping profile; and

associating the vertically discretized doping profile with an access key, the access key comprising a region name and a cross-section name.

9. A computer-readable medium, the computer-readable medium storing thereon computer readable instructions for characterizing an integrated circuit substrate, comprising:

instructions for obtaining a substrate doping profile, the substrate doping profile including a net doping level for each one of a plurality of depths within the integrated circuit substrate;

instructions for vertically discretizing the substrate doping profile to form a vertically discretized substrate doping profile; and

instructions for associating the vertically discretized doping profile with an access key, the access key corresponding to a region of the integrated circuit substrate and a cross-section of the integrated circuit substrate.

10. The computer-readable medium as recited in claim 9, wherein the access key is associated with a region name and a cross-section name.

11. The computer-readable medium as recited in claim 9, wherein the access key comprises a region name and a cross-section name.

12. The computer-readable medium as recited in claim 9, wherein the region is an area of the integrated circuit substrate in which a number of transitions between p-type material and n-type material within bulk underlying the region is approximately constant within the region.

13. The computer-readable medium as recited in claim 9, wherein the region is an area of the integrated circuit substrate in which vertical locations of transitions between p-type material and n-type material within bulk underlying the region are approximately constant within the region.

14. The computer-readable medium as recited in claim 9, wherein the cross-section of the integrated circuit substrate is a default cross-section of the integrated circuit substrate when no specific cross-section is indicated.

15. The computer-readable medium as recited in claim 9, wherein the region of the integrated circuit substrate is a default region of the integrated circuit substrate when no specific region is indicated.

16. The computer-readable medium as recited in claim 9, further comprising:

instructions for determining from the access key whether to add a junction capacitance.

17. An apparatus for characterizing an integrated circuit substrate, comprising:

a processor; and

a memory, at least one of the processor and the memory being adapted for:

obtaining a substrate doping profile, the substrate doping profile including a net doping level for each one of a plurality of depths within the integrated circuit substrate;

vertically discretizing the substrate doping profile to form a vertically discretized substrate doping profile; and

associating the vertically discretized doping profile with an access key, the access key corresponding to a region of the integrated circuit substrate and a cross-section of the integrated circuit substrate.

18. The apparatus as recited in claim 17, wherein the access key is associated with a region name and a cross-section name.

19. The apparatus as recited in claim 17, wherein the access key comprises a region name and a cross-section name.

20. An apparatus for characterizing an integrated circuit substrate, comprising:

means for obtaining a substrate doping profile, the substrate doping profile including a net doping level for each one of a plurality of depths within the integrated circuit substrate;

means for vertically discretizing the substrate doping profile to form a vertically discretized substrate doping profile; and

means for associating the vertically discretized doping profile with an access key, the access key corresponding to a region of the integrated circuit substrate and a cross-section of the integrated circuit substrate.

Please **CANCEL** claim 1.

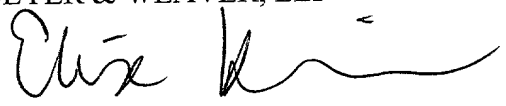
REMARKS

Claim 1 has been cancelled and claims 2-20 have been added. Claims 2-20 remain pending. Reconsideration of the application and an early Notice of Allowance are earnestly solicited.

If there are any issues remaining which the Examiner believes could be resolved through either a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for an extension of time which may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in connection with the filing of this Amendment is to be charged to Deposit Account No. 50-0388 (Order No. SNTCP001X2C1)

Respectfully submitted,
BEYER & WEAVER, LLP



Elise R. Heilbrunn
Reg. No. 42,649

BEYER & WEAVER, LLP
P.O. Box 778
Berkeley, California 94704-0778
Tel. (510) 843-6200